a pulse-width modulator, arranged for generating a pulse-width modulated version of an applied input image signal, based on the clock signal outputted by said clock generator; and

an image forming member, arranged to form an image based on the pulse-width modulated version of the applied input image signal, generated by said pulse-width modulator.

50. (New) A method for forming an image, comprising the steps of:

operating a clock generator that includes a plurality of serially-coupled flip-flops to sequentially output, from the clock generator, successive data collectively forming a clock signal;

generating a pulse-width modulated version of an applied input image signal, based on the clock signal outputted by the clock generator; and

forming an image based on the pulse-width modulated version of the applied input image signal, generated in the generating step.

REMARKS

Claims 35-50 are now pending in this application. Claims 35 and 46-50 are independent claims. Claims 49 and 50 have been added to provide Applicant with a more complete scope of protection.

In the Office Action, Claims 35-48 were rejected under 35 U.S.C. § 103(a) as being obvious from European Patent Specification 0 421 712 B1 (Ojima et al.).

Independent Claim 35 is directed to an image forming apparatus comprising an image forming member adapted to form an image, and a pulse-width modulation means for generating a pulse-width modulation signal in accordance with an image signal. The pulse-width modulation means generates the pulse-width modulation signal by counting pulses of a first clock signal in accordance with the image signal, and the first clock signal is generated by reading data from a storage means which stores output pattern data of the first clock signal. The reading of data from the storage means is performed by outputting data corresponding to the pattern data from a plurality of flip-flops connected in series, and the flip-flops latch the pattern data of the first clock signal.

According to an aspect of the invention recited in Claim 35, pattern data corresponding to a clock pattern is stored in advance, and a desired clock signal pattern is generated by outputting bit data from a plurality of flip-flops connected in series, wherein the flip-flops store the pattern data.

Independent Claims 46-48 are electron beam apparatus, modulation circuit, and method claims, respectively, which each recite features that correspond in many respects to those of independent Claim 35 discussed above.

Independent Claims 49 is directed to an image forming apparatus comprising a clock generator including a plurality of serially-coupled flip-flops that are operable as shift registers for sequentially outputting data forming a clock signal from the clock generator, a

pulse-width modulator, arranged for generating a pulse-width modulated version of an applied input image signal, based on the clock signal outputted by the clock generator, and an image forming member, arranged to form an image based on the pulse-width modulated version of the applied input image signal, generated by the pulse-width modulator.

Independent Claim 50 is a method claim corresponding to apparatus Claim 49.

Ojima et al. refers to pulse-width modulating an eight bit input image signal into an output signal OPD whose minimum pulse width is 1/4 the period of the input image signal VDO. A master clock CLK has a frequency which is the same as that of the input signal VDO, and switching clocks SCLK1 and SCLK2 having periods that are ½ of the period of the master clock CLK are generated. Up/down counters 8 and 9 receive the switching clocks SCLK1 and SCLK2, respectively. The counters 8 and 9 are counted up or down in synchronization with the switching clocks SCLK1 and SCLK2, respectively, and outputs of the counters 8 and 9 are latched and then delivered to comparators 4 and 5, respectively. Input image data VDO is compared by the comparators 4 and 5, and the results are then forwarded to latches 13 and 14, respectively. Items of image data D1, D2 obtained from latches 13 and 14 enter a changeover circuit 15 where they are alternately selected in successive fashion based on the switching clocks SCLK1, SCLK2, and the successively selected items of data are outputted as serial output image data OPD. The circuit 15 includes a J-K flip-flop 17, AND gates 18, 19, and an OR gate 20. When signal

SCLK2 rises, the image data D1 is outputted as the output image data OPD, and thus the serial image data OPD is delivered in an order decided by the latching of latches 13 and 14.

Applicant respectfully submits that, while Ojima et al. may refer to the foregoing features, nothing in that reference would teach or suggest generating a pulse-width modulation signal by counting pulses of a first clock signal in accordance with an image signal, *wherein the first clock signal is generated by outputting data corresponding to pattern data from a plurality of flip-flops connected in series, and the flip-flops latch the pattern data of the first clock signal*, as recited in Claims 35 and 46-48, or operating a clock generator including a plurality of serially-coupled flip-flops to sequentially output data forming a clock signal from the clock generator, and generating a pulse-width modulated version of an applied input image signal, based on the clock signal outputted by the clock generator, as recited in Claims 49 and 50.

The Office Action concedes that Ojima et al. does not teach or suggest "a plurality of flip-flops latching the pattern data", but then alleges that "it would have been obvious to one of ordinary skill in the art to utilize a plurality of connected in series flip-flops [in lieu of the single flip-flop 17 shown in Fig. 3] as to latch the pattern data of the first clock signal because it would provide a simply constructed image forming apparatus . . . ." However, since a plurality of serially-connected flip-flops would seemingly be a more complex structure than a single flip-flop 17, one skilled in the art would not have been motivated to replace that single flip-flop 17 with such a structure, especially since col. 4, lines 52-54 of Ojima et al. explicitly describes a need to provide a simply constructed image

forming apparatus, and thus appears to teach away from replacing the single flip-flip 17 with a more complex configuration (such as a plurality of series-connected flip-flops). Moreover, although the Office Action asserts that "A plurality of flip-flops is very well known in the art and Ojima could have used more than one flip-flop to carry out his invention", it is well established that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggest the desirability of the combination." MPEP 2143.01 (citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)). For the reason given above and the for reasons given from page 4, line 14 to page 5, line 4 of the Request For Reconsideration filed on April 25, 2001 (which pages are incorporated by reference herein), Applicant respectfully asserts that one skilled in the art would not have been motivated to modify Ojima et al. in the manner proposed in the Office Action.

Furthermore, even assuming *arguendo* if the flip-flop 17 of Ojima et al. were to be replaced with a plurality of serially-connected flip-flops, as proposed in the Office Action, the result would merely be a series of flip-flops which would seemingly cause the opening/closing of AND gates 18 and 19 of the changeover circuit 15 (Fig. 3), for causing the alternate outputting of data D1 or D2 as data OPD – not a pulse-width modulator for generating a pulse-width modulated signal based on a clock signal formed by data outputted using a plurality of serially-connected flip-flops, as recited in Claims 35 and 46-50. Indeed, the flip-flop 17 of Ojima et al. is not seen to be provided for generating a desired clock pattern, but instead merely causes the alternate selection of data D1 or D2, based on two

previously generated clock signals SCLK1 and SCLK2 that are inverted relative to one another.

For all of the foregoing reasons, Applicant respectfully submits that it would not have been obvious to one skilled in the art at the time of Applicant's invention to modify Ojima et al. as proposed in the Office Action, in an attempt to attain Applicant's invention as defined in Claims 35 and 46-50. Accordingly, Claims 35 and 46-50 are each deemed clearly patentable over Ojima et al.

If, after considering the foregoing remarks, the Examiner still maintains the same prior art rejection of the pending claims in a next Office Action, he is respectfully requested to point out (1) why he believes that one skilled in the art would have been motivated to replace the single flip-flop 17 of Ojima et al. with the more complex structure of a plurality of serially-connected flip-flops, when Ojima et al. seemingly teaches away from employing such a more complex structure, and (2) why the Examiner believes that such a replacement would generate a clock signal used to generate a pulse-width modulated signal, when the flip-flop 17 of Ojima et al. merely causes data D1 or D2 to be alternately selected based on two previously generated clock signals SCLK1 and SCLK2.

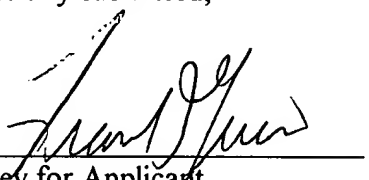
A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as a reference against the independent claims herein. Those claims are therefore believed patentable over the art of record.

The other claims in this application are each dependent from independent Claim 38, discussed above, and are therefore believed patentable for the same reasons as is Claim 38. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of each on its own merits is respectfully requested.

This Amendment After Final Action is believed clearly to place this application in condition for allowance and its entry is therefore believed proper under 37 C.F.R. § 1.116. The added independent claims are similar in scope to the other independent claims of this application. In any event, however, entry of this Amendment After Final Action, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested. Should the Examiner believe that issues remain outstanding, he is respectfully requested to contact Applicant's undersigned attorney in an effort to resolve such issues and advance the case to issue.

Applicant requests favorable consideration and an early Notice of Allowance in the present application.

Respectfully submitted,



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